University of Mosul

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FPGA Based STFT Analysis For EEG Task Classification

By

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ABSTRACT

Recent advances in computer hardware and signal processing have made the use of Electroencephalography EEG signals or brain waves possible for communication between humans and machines.

The EEG signal carries information and features for the mental state of the brain. In this thesis, the EEG signals with no feature extraction(Time Domain), with frequency analysis, with Time-Frequency Analysis and with Time-Frequency-space Analysis are used for EEG classification. EEG signals for four subjects recorded from 16 channels have been studied during several mental and motor tasks.

A back propagation neural network classifier is used for EEG signals classification. The extracted features are fed to several neural network layouts and tested to find a layout that gives good classification rate as well as a lower number of multipliers and gates to be suitable for hardware implementation. It is found that two hidden layers network gives better performance than one hidden layer with bigger number of neurons.

Classification rate that reaches 100% between two tasks and 96% between three tasks using Space-Time-Frequency-analysis and Time-Frequency-analysis was obtained and it is found that the following electrode pairs gives the best classification rates in general(*Fp2- F4*, *F4 - C4, C4- P4, Fp1- F3, F3 - C3*). Results show that four electrodes is very sufficient to achieve good classification results between two or three tasks, so lower number of electrodes is sufficient.

The second part of the work is the FPGA based hardware implementation of the Short Time Fourier Transform (STFT) which is the Time-Frequency Analysis tool that is chosen to extract the EEG features. The STFT structure is implemented based on the FFT algorithm.

Experimental and simulation results are provided within this project. The STFT architecture are implemented using *VHDL* programming language that is created and simulated with the aid of the *ISE 9.2* simulator.

The implementation of the designed STFT structure using the *FPGA SPARTAN-3E* kit utilize 72% of the available slices. the EEG data are represented using 16 bits. The speed up of the designed hardware over the software that is executed using a general purpose processor operating at 2GHz with 1GB RAM is equal to 1570.

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